

LIN-bus ESD protection diode

1. Product profile

1.1 General description

SLPESD1LIN is a very small SOD323 (SC-76) Surface-Mounted Device (SMD) plastic package designed to protect one automotive Local Interconnect Network (LIN) bus line from the damage caused by ElectroStatic Discharge (ESD) and other transients.

1.2 Features and benefits

- ESD protection of one automotive LIN-bus line
- Asymmetrical diode configuration ensures an optimized protection against ElectroMagnetic Interferences (EMI) of a LIN Electronic Control Unit (ECU)
- Max. peak pulse power: $P_{PP} = 160 \text{ W}$ at $t_p = 8/20 \mu\text{s}$
- Low clamping voltage: $V_{CL} = 40 \text{ V}$ at $I_{PP} = 1 \text{ A}$
- Ultra low leakage current: $I_{RM} < 1 \text{ nA}$
- ESD protection of up to 23 kV
- IEC 61000-4-2, level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{PP} = 3 \text{ A}$ at $t_p = 8/20 \mu\text{s}$

1.3 Applications

- LIN-bus protection
- Automotive applications

1.4 Quick reference data


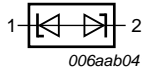
Table 1. Quick reference data

$T_{amb} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage					
	SLPESD1LIN(15 V)		-	-	15	V
	SLPESD1LIN(24 V)		-	-	24	V
C_d	diode capacitance	$V_R = 0 \text{ V};$ $f = 1 \text{ MHz}$	-	13	17	pF

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode 1 (15 V)		 006aab04
2	cathode 2 (24 V)		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
SLPESD1LIN	SC-76	plastic surface-mounted package; 2 leads	SOD323

4. Marking

Table 4. Marking codes

Type number	Marking code
SLPESD1LIN	AM

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{PP}	peak pulse power	$t_p = 8/20 \mu s$	[1] -	160	W
I_{PP}	peak pulse current	$t_p = 8/20 \mu s$	[1] -	3	A
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	+150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

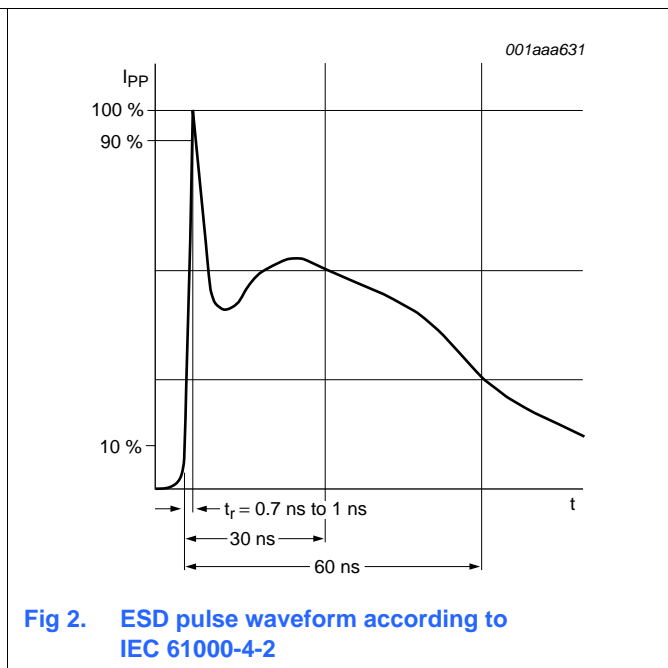
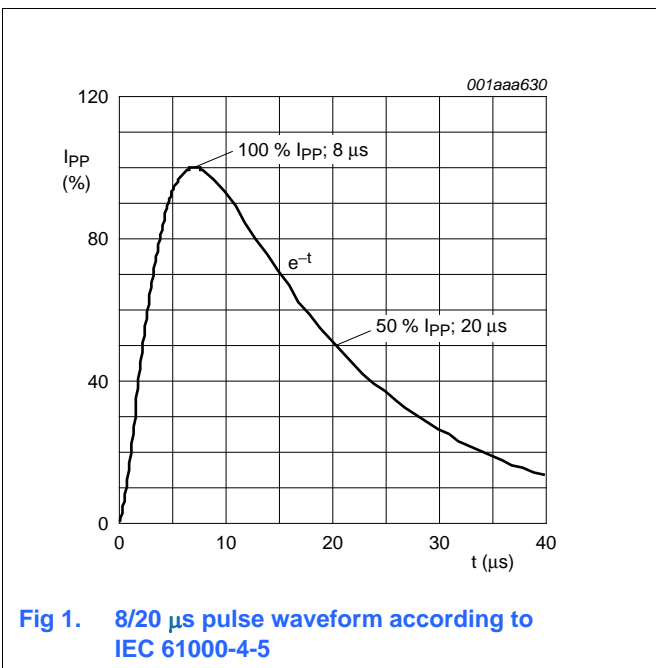
Table 6. ESD maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	1] -	23	kV
		MIL-STD-883 (human body model)	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

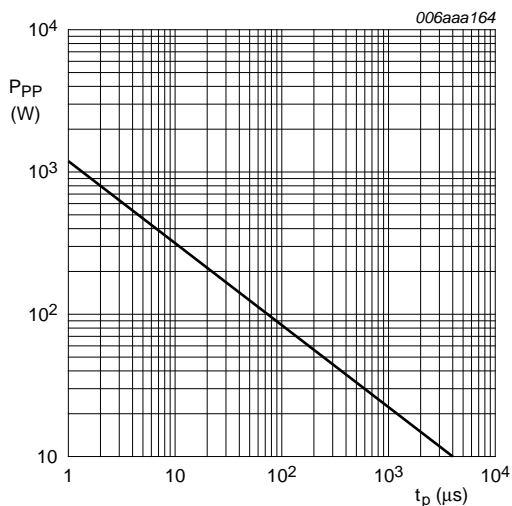


6. Characteristics

Table 8. Characteristics
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage					
	SLPESD1LIN(15 V)		-	-	15	V
	SLPESD1LIN(24 V)		-	-	24	V
I _{RM}	reverse leakage current					
	SLPESD1LIN(15 V)	V _{RWM} = 15 V	-	< 1	50	nA
	SLPESD1LIN(24 V)	V _{RWM} = 24 V	-	< 1	50	nA
V _{BR}	breakdown voltage	I _R = 5 mA				
	SLPESD1LIN(15 V)		17.1	18.9	20.3	V
	SLPESD1LIN(24 V)		25.4	27.8	30.3	V
C _d	diode capacitance	V _R = 0 V; f = 1 MHz	-	13	17	pF
V _{CL}	clamping voltage		[1]			
	SLPESD1LIN(15 V)	I _{PP} = 1 A	-	-	25	V
		I _{PP} = 5 A	-	-	44	V
	SLPESD1LIN(24 V)	I _{PP} = 1 A	-	-	40	V
		I _{PP} = 3 A	-	-	70	V
r _{dif}	differential resistance					
	SLPESD1LIN(15 V)	I _R = 1 mA	-	-	225	Ω
	SLPESD1LIN(24 V)	I _R = 1 mA	-	-	300	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.



T_{amb} = 25 °C

Fig 3. Peak pulse power as a function of exponential pulse duration; typical values

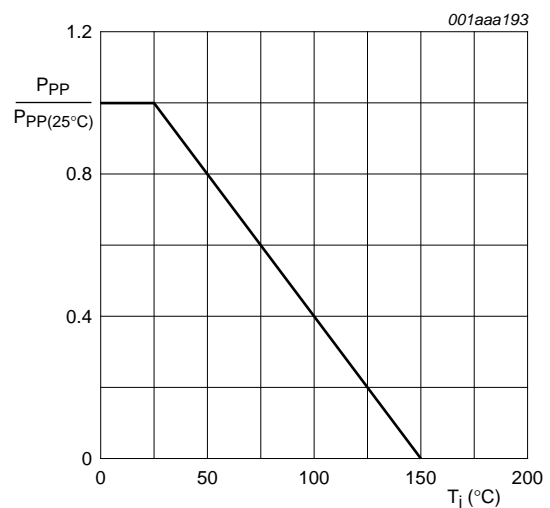


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values

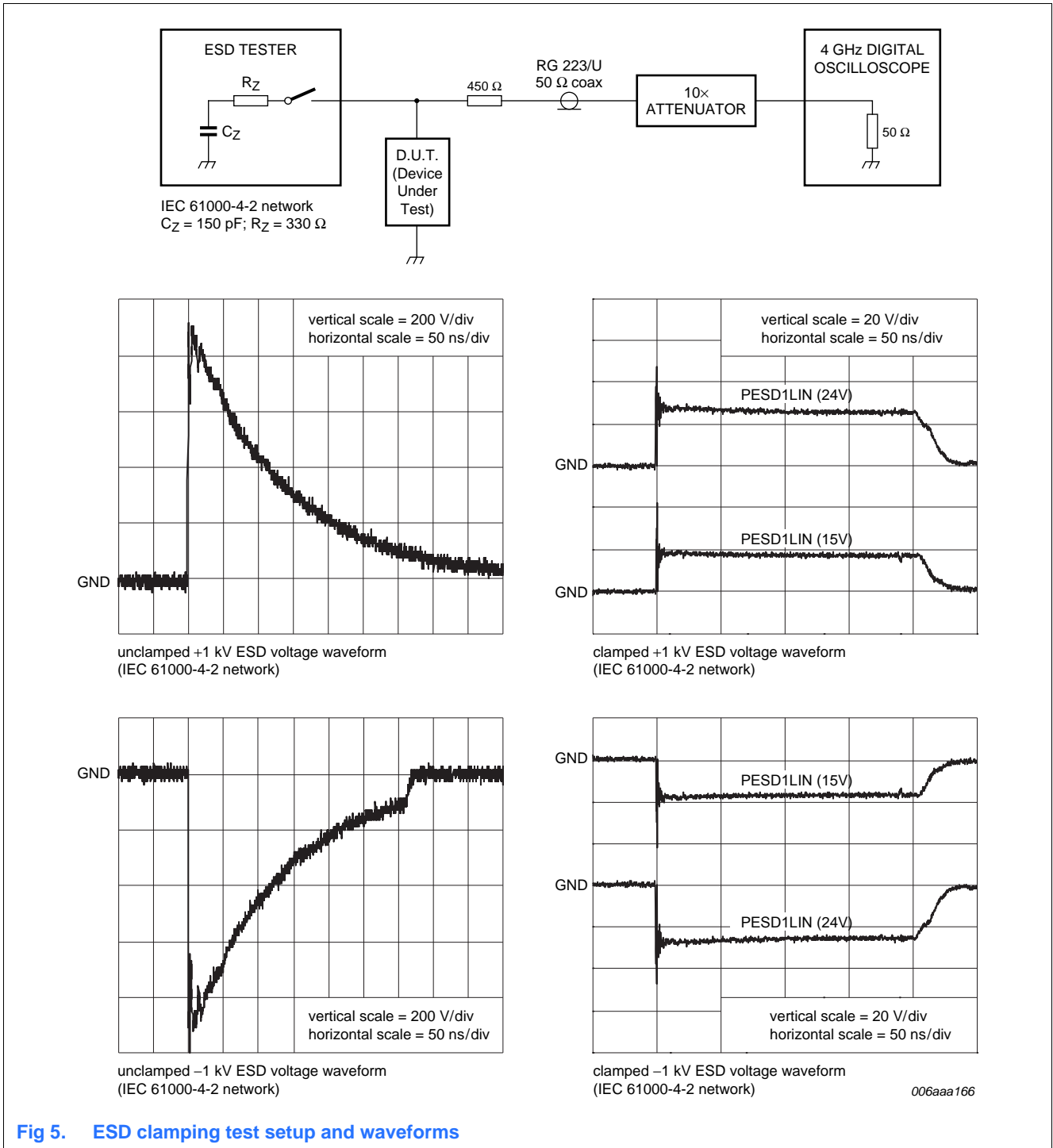


Fig 5. ESD clamping test setup and waveforms

7. Application information

The SLPESD1LIN is designed for the protection of one LIN-bus signal line from the damage caused by ESD and surge pulses. The SLPESD1LIN provides a surge capability of up to 160 W per line for a 8/20 μ s waveform.

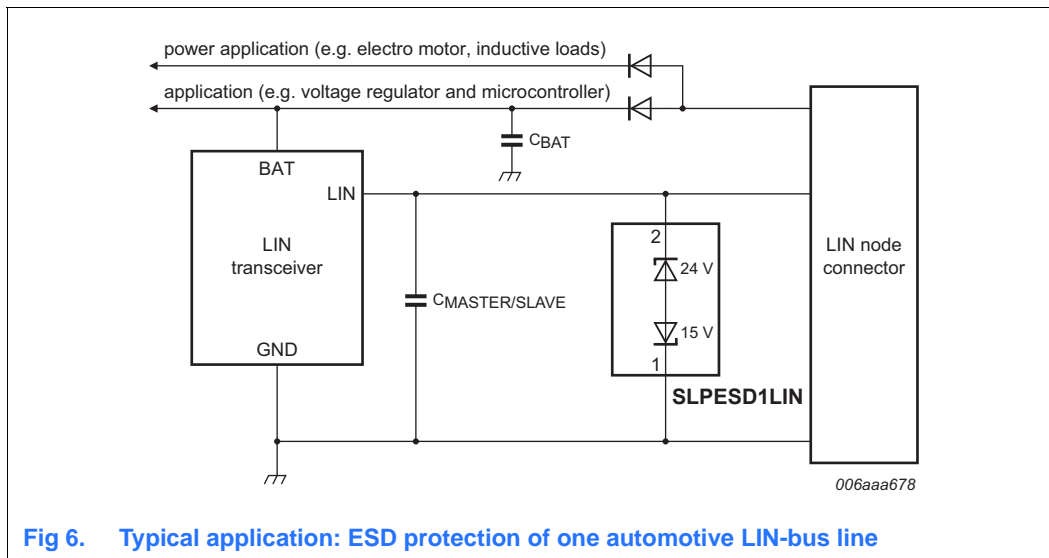


Fig 6. Typical application: ESD protection of one automotive LIN-bus line

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the SLPESD1LIN as close to the input terminal or connector as possible.
2. The path length between the SLPESD1LIN and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protection conductors in parallel with unprotected conductor.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

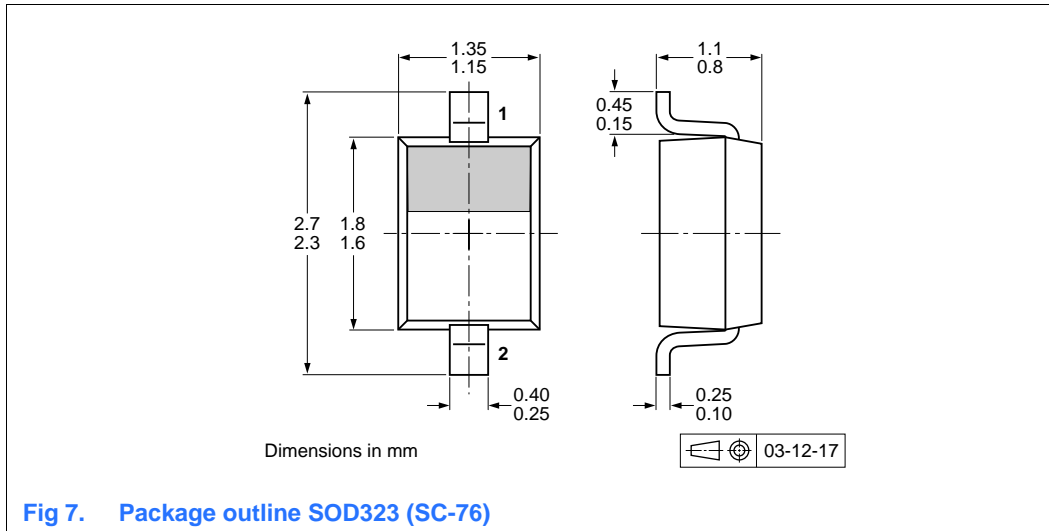


Fig 7. Package outline SOD323 (SC-76)